

WHAT IS CLAIMED IS:

1. An apparatus for generating an interrupt, said
2 interrupt being requested by an assertion of an interrupt
3 request signal, and said apparatus comprising:
4 means for indicating a software condition;
5 means for indicating a hardware condition; and
6 means for generating said interrupt in response to
7 the assertion of said interrupt request signal, said
8 means for generating responsive to said software
9 condition and said hardware condition.

1. An apparatus as recited in claim 1 wherein said
2 means for generating generates said interrupt when said
3 interrupt request is asserted and said hardware condition
4 is indicated, regardless of said software condition.

1 3. An apparatus as recited in claim 2 wherein said
2 means for generating comprises:
3 means for enabling said interrupt in response to
4 said software condition and said hardware condition; and
5 means for asserting said interrupt when said
6 interrupt request is asserted and said interrupt is
7 enabled and for not asserting said interrupt when said
8 interrupt request is asserted and said interrupt is not
9 enabled.

1 *Sub E3* 4. An apparatus as recited in claim 3 wherein said
2 means for indicating said software condition comprises a
3 programmable register that outputs a software enable
4 signal.

1 5. An apparatus as recited in claim 4 wherein said
2 means for indicating said hardware condition comprises at
3 least one hardware circuit, and wherein each of said at
4 least one hardware circuit outputs a hardware enable
5 signal.

1 *Sub E4* 6. An apparatus as recited in claim 5 wherein said
2 means for enabling said interrupt comprises an OR gate
3 that receives said software enable signal and said
4 hardware enable signal and that outputs a combined enable
5 signal.

1 *Sub E5* 7. An apparatus as recited in claim 6 wherein said
2 means for asserting comprises an AND gate that receives
3 said combined enable signal and said interrupt request
4 signal and that outputs said interrupt.

1 8. An apparatus as recited in claim 7 wherein said
2 apparatus is included in a processor, and wherein said at
3 least one hardware circuit asserts said hardware enable
4 signal when said processor is in a particular state.

1 ⁶ 9. An apparatus as recited in claim ⁵ 8 wherein said
2 particular state comprises an idle mode.

1 ^{Sub} ⁶ 10. An apparatus as recited in claim 7 wherein said
2 apparatus is included in a processor, and wherein said at
3 least one hardware circuit asserts said hardware enable
4 signal in response to an external enable signal generated
5 external to said processor.

1 11. An apparatus as recited in claim 8 wherein said
2 at least one hardware circuit further generates said
3 hardware enable signal in response to an external enable
4 signal generated external to said processor.

1 ^{Sub} 12. A method for generating an interrupt, said
2 interrupt being requested by the assertion of an
3 interrupt request signal, said method comprising the
4 steps of:

5 indicating a hardware condition;
6 indicating a software condition; and
7 generating said interrupt in response to said
8 interrupt request signal, said step of generating
9 dependent upon said software condition and said hardware
10 condition.

1 13. A method as recited in claim 12, wherein said
2 step of generating comprises the step of generating said

3 interrupt when said interrupt request is asserted and
4 said hardware condition is indicated, regardless of said
5 software condition.

1 14. A method as recited in claim 13, wherein said
2 step of generating comprises the steps of:

3 enabling said interrupt in response to said software
4 condition and said hardware condition; and

5 asserting said interrupt when said interrupt request
6 is asserted and said interrupt is enabled, and not
7 asserting said interrupt when said interrupt request is
8 asserted and said interrupt is not enabled.

1 15. A method as recited in claim 14, wherein said
2 step of indicating said software condition is performed
3 by a programmable register that outputs a software enable
4 signal.

1 16. A method as recited in claim 15, wherein said
2 step of indicating said hardware condition is performed
3 by at least one hardware circuit, and wherein each of
4 said at least one hardware circuit outputs a hardware
5 enable signal.

1 17. A method as recited in claim 16, wherein said
2 step of enabling said interrupt is performed by an OR
3 gate that receives said software enable signal and said

4 hardware enable signal and that outputs a combined enable
5 signal.

1 18. A method as recited in claim 17, wherein said
2 step of asserting is performed by an AND gate that
3 receives said combined enable signal and said interrupt
4 request signal and that outputs said interrupt.

1 19. A method as recited in claim 18, wherein said
2 interrupt is received by a processor, and wherein said at
3 least one hardware circuit asserts a hardware enable
4 signal when said processor is in a particular state.

1 20. A method as recited in claim 19, wherein said
2 particular state is an idle mode.

1 21. A method as recited in claim 18, wherein said
2 interrupt is received by a processor, and wherein said at
3 least one hardware circuit asserts said hardware enable
4 signal in response to an external enable signal generated
5 externally of said processor.

1 22. A method as recited in claim 19 wherein said at
2 least one hardware circuit further generates said
3 hardware enable signal in response to an external enable
4 signal generated externally of said processor.

Add A3^{D5}